**Part 1: Multiple choice question**

1. When a cache is full and a new cache line needs to be fetched into it, which of the following is a pretty good, practical approach?

A. randomly selecting a cache location for the new line.

B. choosing the cache location currently occupied by the least-recently-used data.

C. choosing always the same cache location for the new line.

D. denying the memory operation that caused the fetch of the new line.

1. About the cache in a computer system, which is true
2. Every computer system has 3 level cache, that is L1, L2, L3 cache
3. Every computer systems' cache system have data cache and instruction cache
4. Every computer systems' cache system has 2 level cache, that is L1, and L2

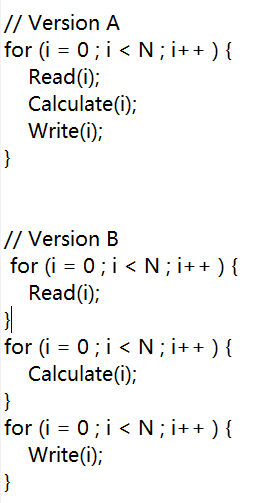
A. II and III only

B. I only

C. I and III only

D. none

1. Consider the following fragments from two versions of a program. Version A Version B as the below pic shown Which of the following are true of version B, compared to version A?



1. B may be faster because of cache effects.
2. B may be slower because of cache effects.
3. B may execute at essentially the same speed as A.

A. II and III only

B. I only

C. I, II, and III

D. I and III only

1. A program whose code and data together occupy fewer than 256 Kbytes is executed on a computer with a 512 Kbyte direct cache. Which of the following is true?

A. No bytes will be fetched from main memory

B. There is no telling, from the information given, how many bytes will be fetched from main memory.

C. Every instruction fetch will cause a cache miss.

D. Some bytes, but at most 256 Kbytes, will be fetched from main memory.

1. Which facts about the cache can be determined by calling the following function? int data[1 << 20];

void callee(int x) {

int i, result;

for (i = 0; i < (1 << 20); i += x) {

result += data[i];

}

}

1. cache line size
2. cache size
3. cache speed

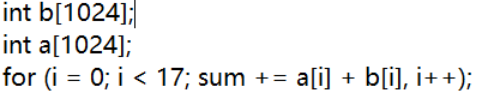
A. I and II only

B. I only

C. I and III only

D. I, II, and III

1. Which is the fastest cache mapping function?
2. Direct mapping
3. Set associative mapping
4. Fully associative mapping
5. All the same.
6. A computer system has a 4KB cache organized in block-set-associative manner with 4 lines per set, 64 bytes per line. The number of bis in the SET and OFFSET fields of the main memory address format is:
7. 4,6
8. 6,4
9. 7,2
10. 15,40
11. Your computer has 32-bit integers and a direct cache containing 128 32-byte cache lines. In the following code fragment, the compiler allocates a at address 0x800000 and b at address 0x801000. Before the execution of the code fragment, the arrays a and b have never been used, so they are not in the cache. What is the minimum number of bytes from each of the arrays a and b that could be fetched into the cache from main memory, during the execution of the code?



A. 68

B. 17

C. 96

D. 1088

1. The principle of locality justifies the use of
2. Interrupt
3. DMA
4. Cache memory
5. Polling
6. Which cache write mechanism allows an updated memory location in the cache to remain out of date in memory until the block containing the updated memory location is replaced in the cache?
7. Write through
8. Write back
9. Both
10. Neither
11. When the following code fragment is executed on a computer with 32-bit integers and a fully-associative cache with 32-byte cache lines, how many bytes of the array a will be fetched into the cache from main memory?

int a[100]; for (i = 0; i < 17; sum += a[i], i++);

A. at most 96.

B. exactly 17.

C. at most 68.

D. exactly 32.

1. Assume a memory access to main memory on a cache "miss" takes 30 ns and a memory access to the cache on a cache "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", what is the average memory access time?
2. 33 nS
3. 27.0 nS
4. 24.6 nS
5. 8.4 nS

**Part 2 : Cache miss rate calculation**

1. Write your solution in a text or Word file and submit it below.

3M decides to make Post-Its by printing yellow squares on white pieces of paper. As part of the printing process, they need to set the CMYK (cyan, magenta, yellow, black) value for every point in the square. 3M hires you to determine the efficiency of the following algorithms on a machine with a 2048-byte direct-mapped data cache with 32-byte blocks. You are given the following definitions:

struct point\_color {  
 int c;  
 int m;  
 int y;  
 int k;  
};

struct point\_color square[16][16];  
 int i, j;

Assume the following:

sizeof(int) == 4.

square begins at memory address 0.

The cache is initially empty.

The only memory accesses are to the entries of the array square. Variables i and j are stored in registers.

Determine the cache performance of the following code:

for(i = 0; i < 16; i++) {  
 for(j = 0; j < 16; j++) {  
 square[i][j].c = 0;  
 square[i][j].m = 0;  
 square[i][j].y = 1;  
 square[i][j].k = 0;  
 }  
}

A. What is the total number of writes?

The total number of writes is 16 x 16 x 4 = 1024  
B. What is the total number of writes that miss in the cache?

The total number of writes that miss in the cache is 16 x 8 = 128  
C. What is the miss rate?

The miss rate is 12.5%

2. Write your solution in a text or Word file and submit it below.

Given the assumptions in Problem 1, determine the cache performance of the following code:

for(i = 0; i < 16; i++) {  
 for(j = 0; j < 16; j++) {  
 square[j][i].c = 0;  
 square[j][i].m = 0;  
 square[j][i].y = 1;  
 square[j][i].k = 0;  
 }  
 }

A. What is the total number of writes?

The total number of writes is 16 x 16 x 4 = 1024  
B. What is the total number of writes that miss in the cache?

The total number of writes that miss in the cache is 16 x 16 = 256  
C. What is the miss rate?

The miss rate is 25%

3. Write your solution in a text or Word file and submit it below.

Given the assumptions in Problem 1, determine the cache performance of the following code:

for(i = 0; i < 16; i++) {  
 for(j = 0; j < 16; j++) {  
 square[i][j].y = 1;  
 }  
}  
for(i = 0; i < 16; i++) {  
 for(j = 0; j < 16; j++) {  
 square[i][j].c = 0;  
 square[i][j].m = 0;  
 square[i][j].k = 0;  
 }  
}

A. What is the total number of writes?

The total number of writes is 1024  
B. What is the total number of writes that miss in the cache?

The total number of writes that miss in the cache is 256  
C. What is the miss rate?

The miss rate is 25%